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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,570	12/05/2003	Marcus D. Riedel	18021-6226	8898

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,570	RIEDEL ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/14/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18,21-46,67,70 and 71* is/are allowed.

6)☒ Claim(s) *1-17,19.20,47-66,68 and 69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003 and 14 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to applicants' Amendment and Remarks filed on 07/14/2006 regarding application 10/728,570 filed on 12/08/2003. Claims 1 – 71 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 47, line 3, before "cyclic parameters" insert —**determined**—.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 13, 15 – 17, 19, 20, 47 – 62, 64 – 66, 68 and 69 are rejected under 35 U.S.C. 102(b) as being unpatentable over applicants' submitted IDS, paper entitled "*Constructive Analysis of Cyclic Circuits*" authored by *Shiple et al.*

5. As to Claim 1, *Shiple et al.* show and teach the following subject matter:

- A combination circuit whose inputs and outputs are defined by a set of equations containing parameters x and y – [Fig. 1; Section 1.1 Well-behaved cyclic circuits]; Notice that (1) x and y are a set of cyclic parameters (2) output of each logic gate (e.g., x for upper gate, y for lower gate) can be defined as a cyclic parameter;
- Building (i.e., synthesizing) combinational circuit...cyclic combinational circuits – [Section 1: Introduction]; Hardware and software synthesis (i.e., logic synthesis process) of cyclic combinational circuits – [title; abstract]; Notice that a

combinational circuit is synthesized in accordance with the cyclic parameters x and y.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claims 47 and 50, reasons are included in **[Response A]** given above.

7. As to Claims 2 – 4 and 51 – 53, in addition to reasons included in **[Response A]** given above, *Shiple et al.* show the following subject matter in equations in Section 1.1 Well-behaved Cyclic Circuits:

- Cyclic parameter y is an input variable to a upper logic gate in Fig. 1(a);
- Cyclic parameter x is an output variable to a upper logic gate in Fig. 1(a);
- Cyclic parameter x is an input variable to a lower logic gate in Fig. 1(a);
- Cyclic parameter y is an output variable to a lower logic gate in Fig. 1(a);
- Two equations, which define a relationship between x and y whereby the relationship includes a cycle;
- Due to the fact that output of each logic gate can be defined as a cyclic parameter, the cyclic parameter can be an internal variable – [Fig. 3];
- There is a structured dependency between an input variable and an output variable – [Fig. 1; Fig. 3].

For reference purposes, the explanations given above in response to Claim 2 – 4 and 51 – 53 are called **[Response B]** hereinafter.

8. As to Claims 5 – 7 and 54 – 56, in addition to reasons **[Response B]** included in given above, *Shiple et al.* show and disclose the subject matter in – [Fig. 1; Fig. 3; Section 1.1]

9. As to Claims 8 – 10, 48, 49 and 57 – 59, in addition to reasons included in **[Response A]** given above, *Shiple et al.* teach the following subject matter:

- Combinational loops (i.e., cyclic loops in cyclic combinational circuits) can be useful...cyclic circuits can be used to *reduce circuit size* – [abstract]. Notice that

the cyclic parameters can be applied in building a *cyclic combinational circuit (building block)* for use in substitution phase of structuring operation of a logic synthesis process in order to *minimize (i.e., optimize) overall size* of a logic circuit under study.

For reference purposes, the explanations given above in response to Claims 8 – 10, 48, 49 and 57 – 59 are called **[Response C]** hereinafter.

10. As to Claims 11, 16, 17, 20, 60, 65, 66 and 69, *Shiple et al.* teach the following subject matter:

- Referring to Fig. 1(a), the cyclic (combinational) circuit is stabilized (i.e., optimized) if both inputs a, b are not 1 – [Section 1.1]; Notice that the cyclic (combinational) circuit is stabilized (optimized) with regard to electrical behavior (i.e., performance);
- Output of the cyclic (combinational) circuit is stabilized for all *wire delay* – [Section 1.1].
- Stabilization of electrical behavior with regard to testability.

11. As to Claims 12, 13, 15, 19, 61, 62, 64 and 68 in addition to stabilize electrical behavior, *Shiple et al.* teach subject matter in **[Response C]** given above regarding reducing (optimizing) circuit size (i.e., area) by using cyclic circuits. Notice that (1) reducing the size is reducing cost of a logic circuit (2) the size of a logic circuit is reduced by reducing a gate count (3) reducing a gate count will minimize power consumption of the logic circuit.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. Claims 14 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' submitted IDS, paper entitled "*Constructive Analysis of Cyclic Circuits*" authored by *Shiple et al.* in view of U.S. Patent No. 5,515,292 to *Roy et al.*

14. As to Claim 14, *Shiple et al.* disclose a combinational circuit is optimized with regard to cost, which is measured as an area (size), they do not teach that the area is determined by literal count. But *Roy et al.* disclose that, in combinational logic (circuit) synthesis, literal count is reduced in order to achieve area saving, which is very important in minimizing the cost of manufacturing a combinational logic circuit – [col. 6, line 53 – col. 7, line 32].

Therefore it would have been obvious at the time the invention was made to a person having ordinary skill to have applied the teachings of *Roy et al.* in reducing literal count of a combinational logic circuit in order to achieve area saving thereby minimizing the cost of manufacturing the combinational logic circuit.

For reference purposes, the explanations given above in response to Claim 14 are called **[Response D]** hereinafter.

15. As to Claim 63, reasons are included in **[Response D]** given above.

Allowable Subject Matter

16. Claims 18, 21 – 46, 67, 70 and 71 are allowed due to allowable subject matter as described in the Office Action mailed 03/14/2006.

Response to Amendment and Remarks

17. Applicants' Amendments & Remarks filed on 07/14/2006 have been reviewed. Applicants' arguments have been fully considered but they are not persuasive. Key argument and its response related to the claims are listed as below:

[Argument]: *Shiple et al.* (Prior Art) doest not teach or suggest synthesizing cyclic combination circuits in accordance with (cyclic) parameters.

[Response]: *Shiple et al.* do teach the following subject matter:

- Cyclic combinational circuits may have well-defined logical and electrical behaviors ...such circuit can be safely in synchronous designs; they appear as the result of ***synthesis*** from synchronous programs written in the Esterel language – [Section 1];
- *Well-behaved cyclic circuits, and x and y (**cyclic parameters**) defined by an equation... a representative of cyclic circuits generated by high-level **synthesis** from languages such as Esterel* – [Section 1.1].

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Sun James Lin* whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday (9:00AM-6:00PM).

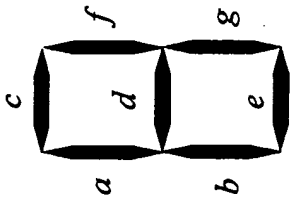
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Jack Chiang* can be reached on (571) 272 - 7483. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308 - 7382 for regular communications and (703) 305 - 3413 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 - 1782.

Sun James Lin
Primary Examiner
Art Unit 2825
September 28, 2006

SUN JAMES LIN
PRIMARY EXAMINER

Reviewed
OK
JR
9-26-06



Inputs				Outputs (corresponding to segments)							
x_3	x_2	x_1	x_0	*a*	*b*	*c*	*d*	*e*	*f*	*g*	display
0	0	0	0	1	1	1	0	1	1	1	**0**
0	0	0	1	0	0	0	0	0	1	1	**1**
0	0	1	0	0	1	1	1	1	1	0	**2**
0	0	1	1	0	0	1	1	1	1	1	**3**
0	1	0	0	1	0	0	1	0	1	1	**4**
0	1	0	1	1	0	1	1	1	0	1	**5**
0	1	1	0	0	1	1	1	1	0	1	**6**
0	1	1	1	0	0	1	0	0	1	1	**7**
1	0	0	0	1	1	1	1	1	1	1	**8**
1	0	0	1	1	0	1	1	0	1	1	**9**

FIGURE 1

(PRIOR ART)

$$f_1 = \bar{x}_3 \bar{f}_2 + \bar{x}_2 x_3$$

$$f_2 = \bar{x}_1 \bar{x}_2 \bar{x}_3 + \bar{x}_1 \bar{f}_3$$

$$f_3 = \bar{x}_1 f_1 + \bar{x}_2 x_3$$

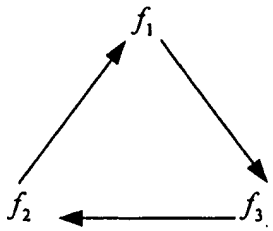


Figure 25